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CENTRAL FAX CENTER****NOV 01 2005****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicants:** Ricky Amos et al. **Examiner:** Matthew C. Landau  
**Serial No.:** 09/995,031 **Art Unit:** 2815  
**Filed:** Herewith **Docket:** YOR920010633US1 (19031)  
**For:** HIGH TEMPERATURE PROCESSING  
COMPATIBLE METAL GATE  
ELECTRODE FOR pFETs AND METHOD  
FOR FABRICATION **Dated:** November 1, 2005

**Confirmation No. 9669**

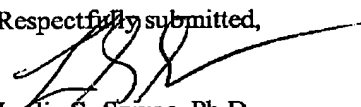
Mail Stop AF  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**SUBMISSION OF EXECUTED DECLARATION PURSUANT TO 37 C.F.R. § 1.131**

Sir:

In applicants' Response dated October 18, 2004, an unexecuted 131 Declaration was filed. Attached herewith is a copy of the executed 131 Declaration. The executed 131 Declaration submitted herein does not include Exhibits A and B which were previously submitted. Applicants hereby submit that the previously submitted Exhibits A and B are applicable here for the executed Declaration and thus respectfully request the Examiner substitute the Exhibits from the previous version for the executed copy attached herewith.

Respectfully submitted,

  
Leslie S. Szivos, Ph.D.  
Registration No. 39,394**CERTIFICATION OF FACSIMILE TRANSMISSION**

I hereby certify that this document is being filed in the United States Patent and Trademark Office on the date shown below via facsimile transmission to Mail Stop Amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 at United States Patent and Trademark Office facsimile transmission number (571) 273-8300.

Dated: November 1, 2005  
Leslie S. Szivos, Ph.D.

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**RECEIVED  
CENTRAL FAX CENTER****NOV 01 2005****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE****Applicant(s):** Ricky Amos, et al.**Examiner:** Matthew C. Landau**Serial No:** 09/995,031**Art Unit:** 2815**Filed:** November 29, 2001**Docket:** YOR920010633US1 (19031)**For:** HIGH TEMPERATURE PROCESSING  
COMPATIBLE METAL GATE ELECTRODE  
FOR pFETs AND METHOD FOR FABRICATION**Dated:** October 18, 2005**Confirmation No:** 9669Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450**DECLARATION PURSUANT TO 37 C.F.R. §1.131**

Sir:

We, Ricky Amos, Douglas A. Buchanan, Cyril Cabral, Jr., Alessandro C. Callegari, Supratik Guha, Hyungjun Kim, Fenton R. McFeely, Vijay Narayanan, Kenneth Rodbell, and John J. Yurkas, hereby declare that:

1. We are co-inventors of the subject matter described and claimed in the above-identified patent application.
2. Prior to August 10, 2001, which is the effective filing date of U.S. Patent No. 6,541,320 to Brown, et al. ("Brown, et al."), we have conceived and reduced to practice a semiconductor structure such as, a metal oxide semiconductor (MOS) or a field effect transistor (FET), that includes a semiconductor substrate having source and drain regions, a gate dielectric having a thickness of less than 100 Å on the semiconductor substrate; and a

gate formed of a metal comprising Re on top of the gate dielectric, as is recited in Claims 1 and 10 of the present application.

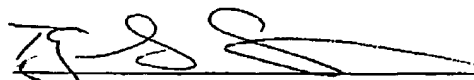
3. As evidence of the conception and reduction to practice of the claimed semiconductor structure referred to in paragraph 2 prior to the effective filing date of Brown, et al., annexed hereto are Exhibits A and B. Exhibit A is a true photocopy of IBM Invention Disclosure YOR820010675, which was created prior to August 10, 2001. Exhibit A includes a Main Ideal section for the Invention Disclosure that describes the fabrication of a semiconductor structure such as a MOS or FET that includes Re as the gate electrode. Exhibit B is the inventors' write-up of the Disclosure that was also created prior to the effective filing date of Brown, et al. This write-up provides greater detail of the invention presently claimed including experimental data that establishes clear evidence of actual fabrication of the claimed semiconductor structure. All names and dates have been redacted in the preparation of this Declaration.

4. We do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

10/18/2005  
Dated

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Dated

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Dated

  
Ricky Amos

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Douglas A. Buchanan

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Cyril Cabral, Jr.

gate formed of a metal comprising Re on top of the gate dielectric, as is recited in Claims 1 and 10 of the present application.

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Dated

Oct 19, 2005

Dated

Dated

Ricky Amos

Douglas A. Buchanan

Douglas A. Buchanan

Cyril Cabral, Jr.

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Dated

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Ricky Amos

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Dated

10/13/05

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Dated

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Douglas A. Buchanan

Cyril Cabral, Jr.

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13 Oct. 2005  
Dated

14 Oct. 2005  
Dated

13 Oct. 2005  
Dated

13<sup>th</sup> October, 2005  
Dated

13<sup>th</sup> October, 2005  
Dated

13<sup>TH</sup> OCT 2005  
Dated

Alessandro C. Callegari  
Alessandro C. Callegari

Supratik Guha  
Supratik Guha

Fenton R. McFeely  
Fenton R. McFeely

Vijay Narayanan  
Vijay Narayanan

Kenneth P. Rodbell  
Kenneth P. Rodbell

John J. Turkas  
John J. Turkas

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Dated

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Alessandro C. Callegari

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Dated

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Supratik Guha

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Dated

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Hyungjun Kim

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Dated

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Fenton R. McFeely

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Dated

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Vijay Narayanan

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Dated

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Kenneth P. Rodbell

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Dated

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John J. Yurkas